IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices

February 1998, ver. 4 Application Note 39

Introduction

As printed circuit boards (PCBs) become more complex, the need for thorough testing becomes increasingly important. Advances in surface-mount packaging and PCB manufacturing have resulted in smaller boards, making traditional test methods—e.g., external test probes and "bed-of-nails" test fixtures—harder to implement. As a result, cost savings from PCB space reductions are sometimes offset by cost increases in traditional testing methods.

In the 1980s, the Joint Test Action Group developed a specification for boundary-scan testing that was later standardized as the IEEE 1149.1-1990 specification. This boundary-scan test (BST) architecture offers the capability to efficiently test components on PCBs with tight lead spacing.

This BST architecture can test pin connections without using physical test probes and capture functional data while a device is operating normally. Boundary-scan cells in a device can force signals onto pins, or capture data from pin or core logic signals. Forced test data is serially shifted into the boundary-scan cells. Captured data is serially shifted out and externally compared to expected results. Figure 1 illustrates the concept of boundary-scan testing.

Figure 1. IEEE 1149.1 Boundary-Scan Testing

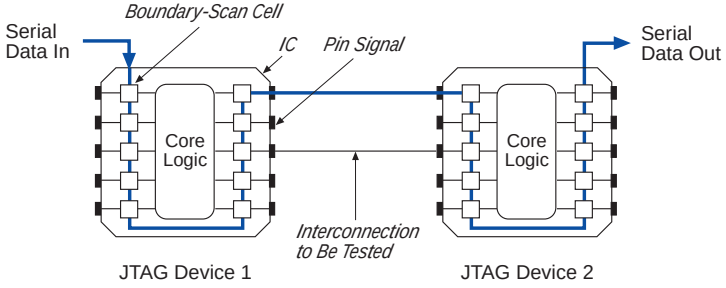


Table 1 summarizes Altera devices that comply with the IEEE 1149.1-1990 specification by providing BST capability for input, output, and dedicated configuration pins.

Table 1. Altera Devices with BST Capability

Family	Devices Supporting BST
FLEX® 10K	All devices
FLEX 8000	EPF8282A, EPF8282AV, EPF8636A, EPF8820A, EPF81500A
FLEX 6000	All devices
MAX® 9000 (including MAX 9000A)	All devices
MAX 7000S *(1)*	EPM7128S, EPM7160S, EPM7192S, EPM7256S
MAX 7000A	All devices

Note:
(1) The EPM7032S, EPM7064S, and EPM7096S devices contain a IEEE 1149.1 controller for in-system programming. However, these devices do not support BST.

This application note discusses using the IEEE 1149.1 BST circuitry in Altera devices. The topics are as follows:

- IEEE 1149.1 BST architecture
- IEEE 1149.1 boundary-scan register
- IEEE 1149.1 BST operation control
- Enabling IEEE 1149.1 BST circuitry
- Guidelines for IEEE 1149.1 boundary-scan testing
- Boundary-Scan Description Language (BSDL) support
- References

In addition to BST, you can use the IEEE 1149.1 controller for in-system programming in MAX 9000 (including MAX 9000A), MAX 7000S, and MAX 7000A devices and for in-circuit reconfiguration in FLEX 10K devices. This application note only discusses the BST feature of the IEEE 1149.1 circuitry.

For more information on using IEEE 1149.1 circuitry for in-system programming and in-circuit reconfiguration, go to the following documents:

- *Application Note 59 (Configuring FLEX 10K Devices)*
- *Application Note 33 (Configuring FLEX 8000 Devices)*
- *Application Note 38 (Configuring Multiple FLEX 8000 Devices)*
- *Application Note 87 (Configuring FLEX 6000 Devices)*
- *Application Note 95 (In-System Programmability in MAX Devices)*

IEEE 1149.1 BST Architecture

A device operating in IEEE 1149.1 BST mode uses four required pins, TDI, TDO, TMS, and TCK, and one optional pin, TRST. Table 2 summarizes the functions of each of the these pins.

Table 2. IEEE 1149.1 Pin Descriptions

Pin	Description	Function
TDI	Test data input	Serial input pin for instructions as well as test and programming data. Data is shifted in on the rising edge of TCK.
TDO	Test data output	Serial data output pin for instructions as well as test and programming data. Data is shifted out on the falling edge of TCK. The pin is tri-stated if data is not being shifted out of the device.
TMS	Test mode select	Input pin that provides the control signal to determine the transitions of the TAP Controller state machine. Transitions within the state machine occur at the rising edge of TCK. Therefore, TMS must be set up before the rising edge of TCK. TMS is evaluated on the rising edge of TCK.
TCK	Test clock input	The clock input to the BST circuitry. Some operations occur at the rising edge, while others occur at the falling edge.
TRST	Test reset input (optional)	Active-low input to asynchronously reset the boundary-scan circuit. This pin is only available in certain FLEX 10K and FLEX 8000 devices (TRST is optional according to IEEE 1149.1).

FLEX 10K and MAX 9000 devices have pins dedicated for IEEE 1149.1 operation. For EPF8820A, EPF8636A, EPF8282A, EPF8282AV, FLEX 6000, and MAX 7000S devices, you can use the four JTAG pins as I/O pins by turning off the JTAG option with the MAX+PLUS II software (see "Enabling IEEE 1149.1 BST Circuitry" on page 241 of this application note). Certain FLEX 10K and FLEX 8000 JTAG devices have the optional pin TRST.

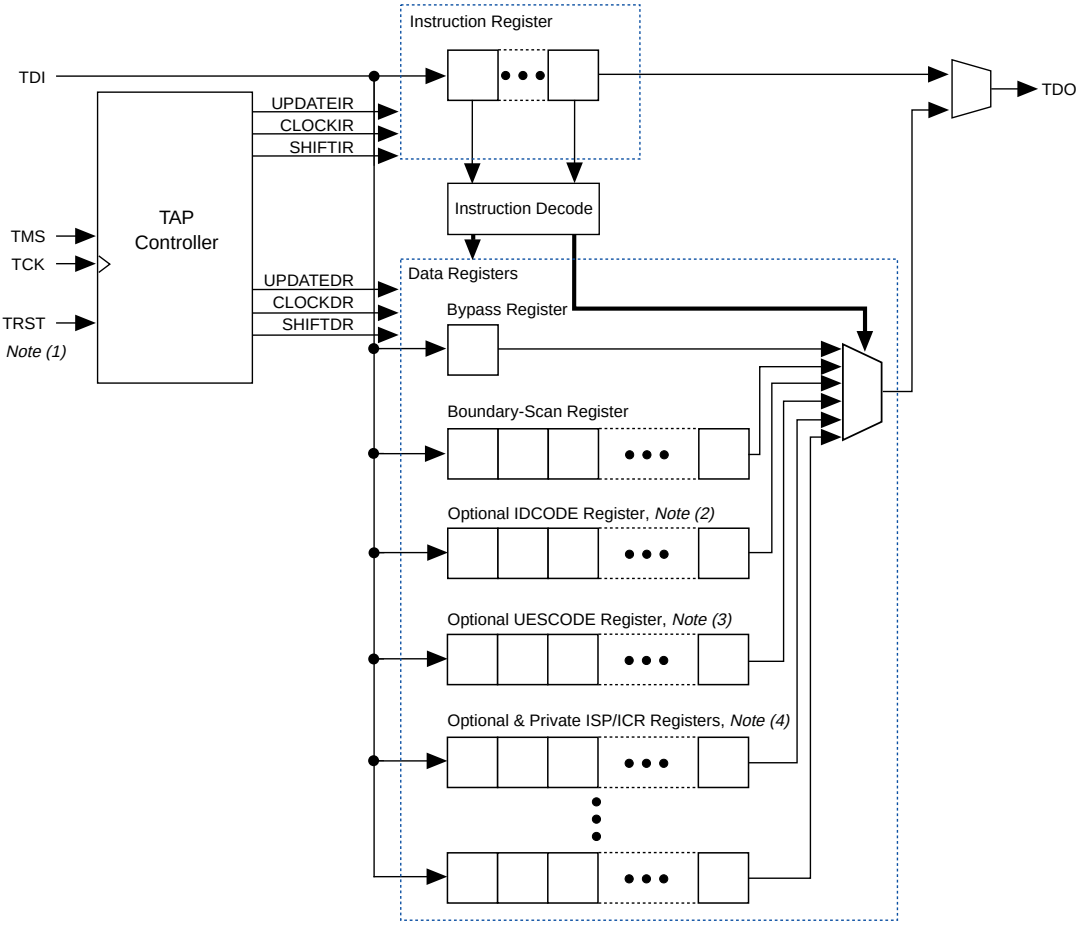
Go to the appropriate device family data sheet for specific device and package combinations.

The IEEE 1149.1 BST requires the following registers:

- The instruction register which is used to determine the action to be performed and the data register to be accessed.
- The bypass register which is a 1-bit-long data register used to provide a minimum-length serial path between TDI and TDO.
- The boundary-scan register which is a shift register composed of all the boundary-scan cells of the device.

Figure 2 shows a functional model of the IEEE 1149.1 circuitry.

Figure 2. IEEE 1149.1 Circuitry



Notes:

(1) The TRST pin is available in some FLEX devices only.

(2) The IDCODE register is available in FLEX 10K, MAX 9000 (including MAX 9000A), MAX 7000A, and MAX 7000S devices.

(3) The UESCODE register is available in FLEX 10K, MAX 7000S, and MAX 9000A devices.

(4) The private registers are used for in-system programmability (ISP) in MAX 9000 (including MAX 9000A), MAX 7000A, and MAX 7000S devices and for in-circuit reconfigurability (ICR) in FLEX 10K devices.

Table 3 shows the length of the instruction register and boundary-scan register for Altera IEEE 1149.1 devices.

Table 3. Length of IEEE 1149.1 Registers

Device	Instruction Register Length (Bits)	Boundary-Scan Register Length (Bits)
EPF10K10, EPF10K10A	10	480
EPF10K20	10	624
EPF10K30, EPF10K30A	10	768
EPF10K40	10	864
EPF10K50, EPF10K50V	10	960
EPF10K70	10	1,104
EPF10K100, EPF10K100A	10	1,248
EPF10K130V	10	1,440
EPF10K250A	10	1,440
EPF8282A, EPF8282AV	3	273
EPF8820A	3	465
EPF6016	3	621
EPF6016A	3	522
EPF6024A	3	681
EPM9320, EPM9320A	10	504
EPM9400	10	552
EPM9480, EPM9480A	10	600
EPM9560, EPM9560A	10	648
EPM7032S, *Note (1)*	10	–
EPM7032A	10	*Note (2)*
EPM7064S, *Note (1)*	10	–
EPM7064A	10	*Note (2)*
EPM7128S, EPM7128A	10	288
EPM7160S	10	312
EPM7192S	10	372
EPM7256S, EPM7256A	10	480
EPM7384A	10	*Note (2)*
EPM7512A	10	*Note (2)*
EPM71024A	10	*Note (2)*

Notes:

(1) This device supports in-system programming through the IEEE 1149.1 interface but does not support BST.

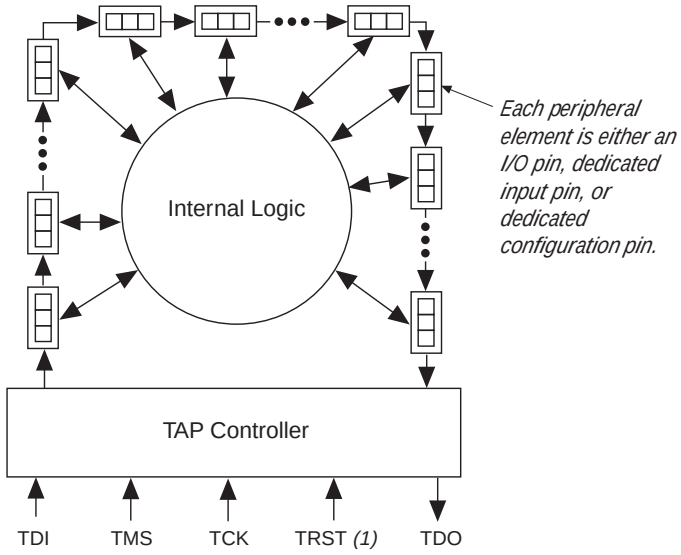
(2) Contact Altera Applications for information on this device.

IEEE 1149.1 boundary-scan testing is controlled by a Test Access Port (TAP) Controller, which is described in "IEEE 1149.1 BST Operation Control" on page 231 of this application note. The TMS, TRST, and TCK pins operate the TAP Controller, and the TDI and TDO pins provide the serial path for the data registers. The TDI pin also provides data to the instruction register, which then generates control logic for the data registers.

IEEE 1149.1 Boundary-Scan Register

The boundary-scan register is a large serial shift register that uses the TDI pin as an input and the TDO pin as an output. The boundary-scan register consists of 3-bit peripheral elements that are either I/O pins (all devices), dedicated inputs (all devices), or dedicated configuration pins (FLEX devices only). You can use the boundary-scan register to test external pin connections or to capture internal data. Figure 3 shows how test data is serially shifted around the periphery of the IEEE 1149.1 device.

Figure 3. Boundary-Scan Register



Note:
(1) The TRST pin is available only in some FLEX devices.

I/O Pin

Figure 4 shows the boundary-scan cells (BSCs) associated with each I/O pin in FLEX 10K, FLEX 8000, and MAX 9000 devices. The 3-bit BSC consists of a set of capture registers and a set of update registers for each I/O pin. The capture registers connect to internal device data via the OUTJ, OEJ, and I/O pin signals, while the update registers connect to external data through the tri-state data input, tri-state control, and INJ signals. The control signals for the IEEE 1149.1 BST registers (e.g., SHIFT, CLOCK, and UPDATE) are generated internally by the TAP Controller; the MODE signal is generated by a decode of the instruction registers. The data signal path for the boundary-scan register runs from the serial data in (SDI) signal to the serial data out (SDO) signal. The scan register begins at the TDI pin and ends at the TDO pin of the device.

Figure 4. FLEX 10K, FLEX 8000 & MAX 9000 I/O Pins with IEEE 1149.1 BST Circuitry

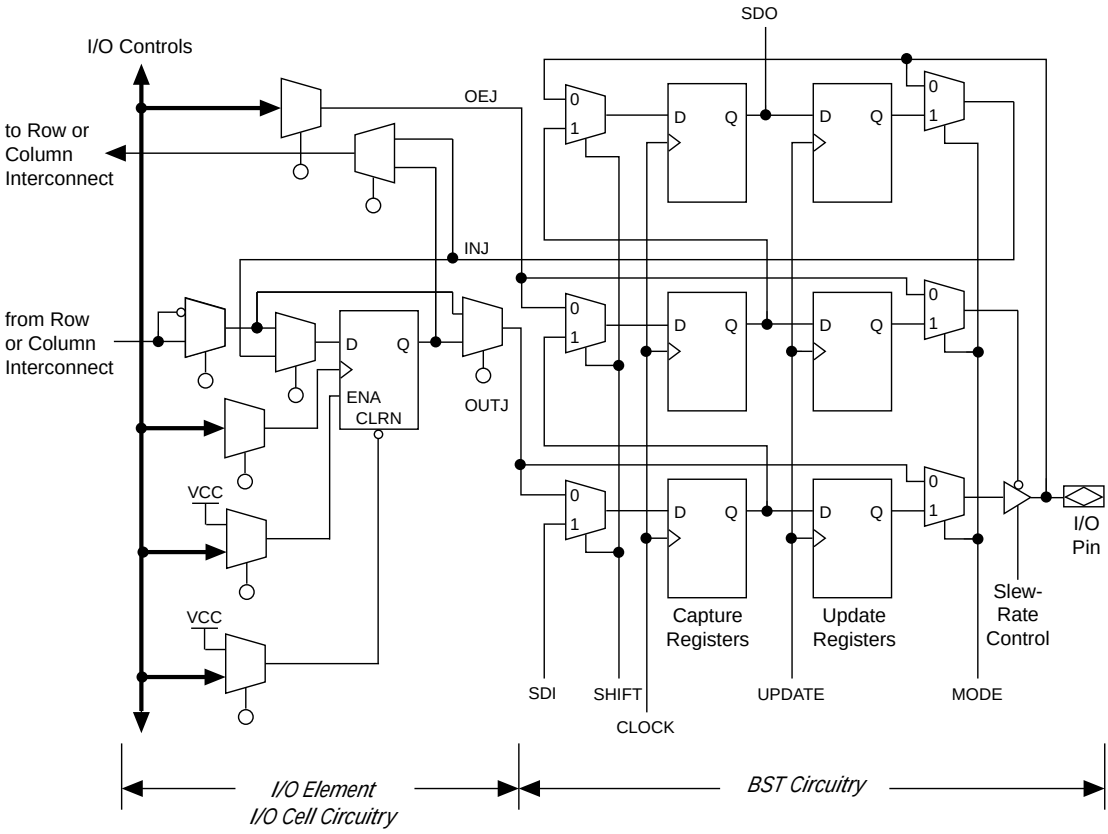


Figure 5 shows the BSCs that are associated with each I/O pin in FLEX 6000 devices.

Figure 5. FLEX 6000 I/O Pins with IEEE 1149.1 BST Circuitry

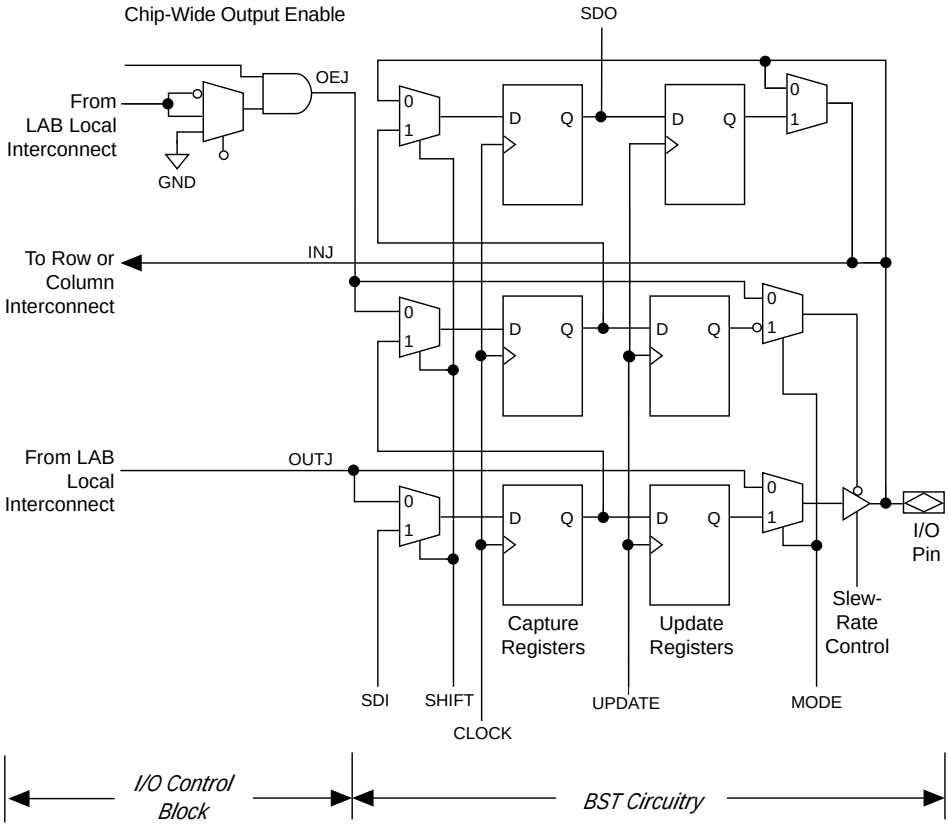
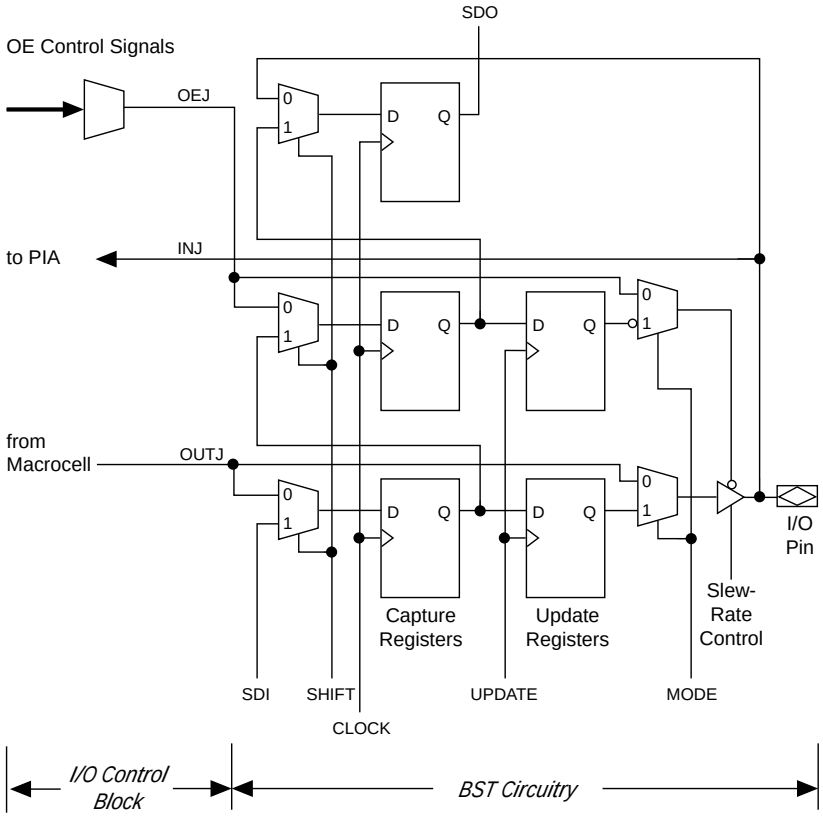


Figure 6 shows the BSCs that are associated with each I/O pin in MAX 7000S and MAX 7000A devices. The BSCs in Figure 6 are similar to BSCs in other device families, except the input portion does not contain an update register.

Figure 6. MAX 7000S & MAX 7000A I/O Pins with IEEE 1149.1 BST Circuitry



Dedicated Input

The boundary-scan register also includes dedicated input pins. Because these pins have special functions, some bits of the boundary-scan register are internally connected to V_{CC} or ground, or used only for device configuration; these bits are thus forced to a static high (1) or low (0) state, or are used internally for configuration.

Figure 7 shows the BSCs for the dedicated input pins in FLEX devices. The register normally associated with an output signal, `OUTJ`, is tied to ground, and the tri-state control, `OEJ`, is connected to V_{CC}. The signal data from the dedicated input is the only register that contains test data. The data shifts out of `SDO` in the order `D`, `1`, and `0`, where `d` is the data associated with the dedicated input. Because only the `D` bit has valid data, a scan test pattern must either ignore or expect the `1` and `0` that follow the `D` bit.

Figure 7. FLEX Dedicated Input Pins with IEEE 1149.1 BST Circuitry

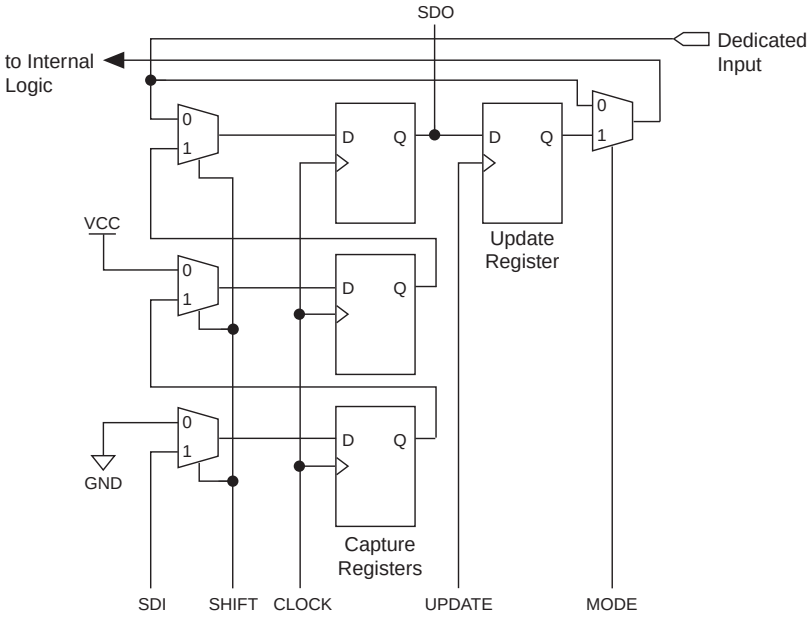
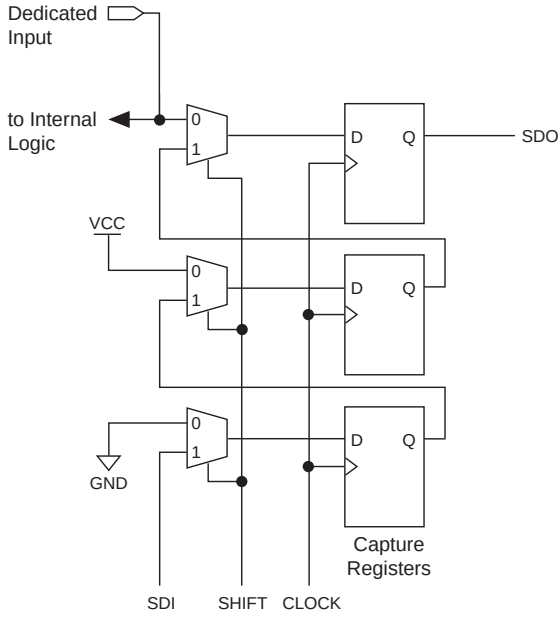


Figure 8 shows the BSCs for the dedicated input pin in MAX devices. All of the update registers in the BSCs are disabled, and the registers normally associated with the output signals OUTJ and OEJ are connected to ground and V_{CC}, respectively. When shifting data in and out of the BSCs, OUTJ and OEJ should be ignored.

Figure 8. MAX Devices Dedicated Input Pins with IEEE 1149.1 BST Circuitry

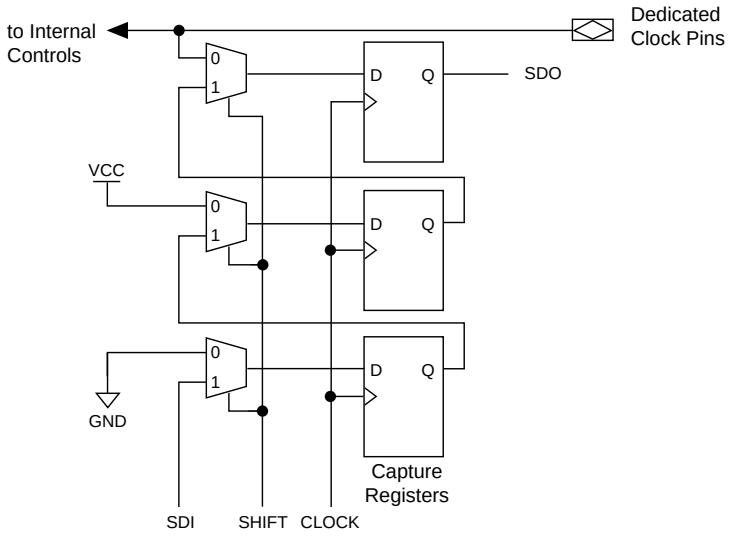


Dedicated Clock Pins (FLEX 10K Only)

The boundary-scan register also includes dedicated clock pins. Because these pins have special functions, some bits of the boundary-scan register are internally connected to VCC or GND configuration; these bits are thus forced to a static high (1) or low (0) state.

Figure 9 shows the BSCs for the dedicated clock pins in FLEX 10K devices. These pins continue to clock internal user registers, but the capture register associated with the pin can be used for external pin connectivity tests. The pin can receive data but cannot force data onto external connections. The data values associated with the other two capture registers should be ignored.

Figure 9. FLEX Dedicated Clock Pins with IEEE 1149.1 BST Circuitry

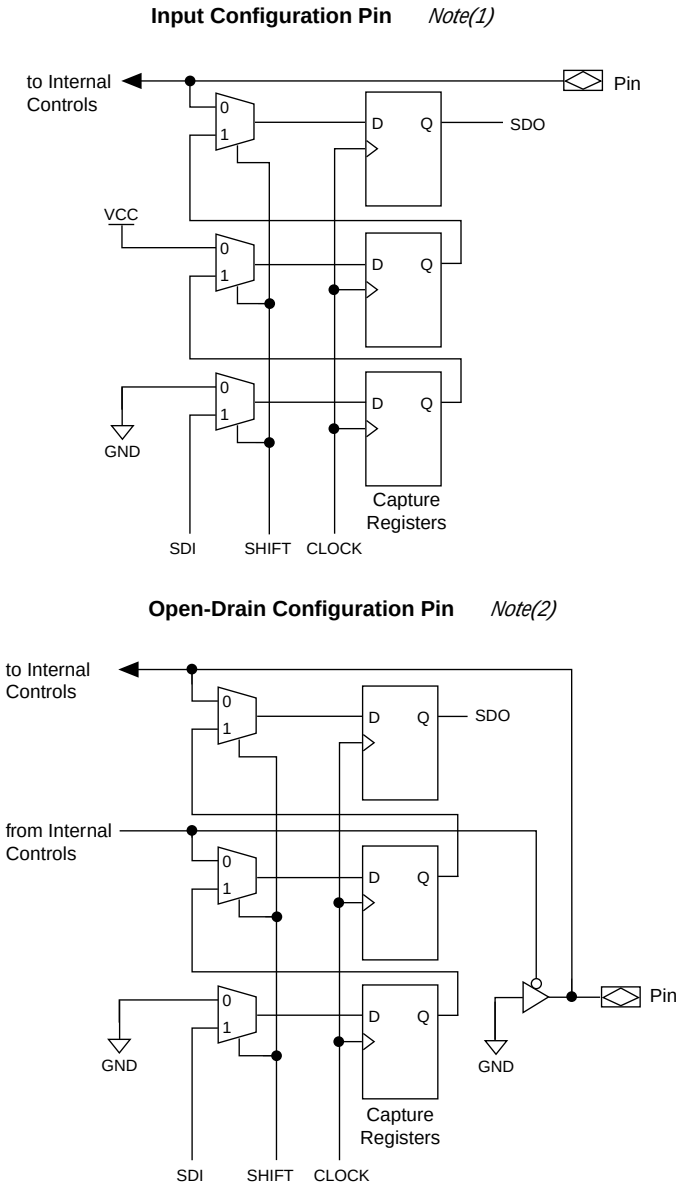


Dedicated Configuration (All FLEX Devices)

The FLEX boundary-scan register includes dedicated configuration pins. Because these pins have special functions, some bits of the boundary-scan register are internally connected to V_{CC} or ground, or are used only for device configuration; these bits are thus forced to a static high (1) or low (0) state, or are used internally for configuration.

Figure 10 shows the peripheral elements associated with the FLEX dedicated configuration pins (i.e., nCONFIG, MSEL0, MSEL1, nSP, CONF_DONE, nSTATUS, and DCLK). These pins are used only during device configuration, but the capture register associated with the pin can be used for external pin connectivity tests. The pin can receive data but cannot force data onto external connections. The data values associated with the other two capture registers should be ignored.

Figure 10. FLEX Dedicated Configuration Pins with IEEE 1149.1 BST Circuitry (Part 1 of 2)

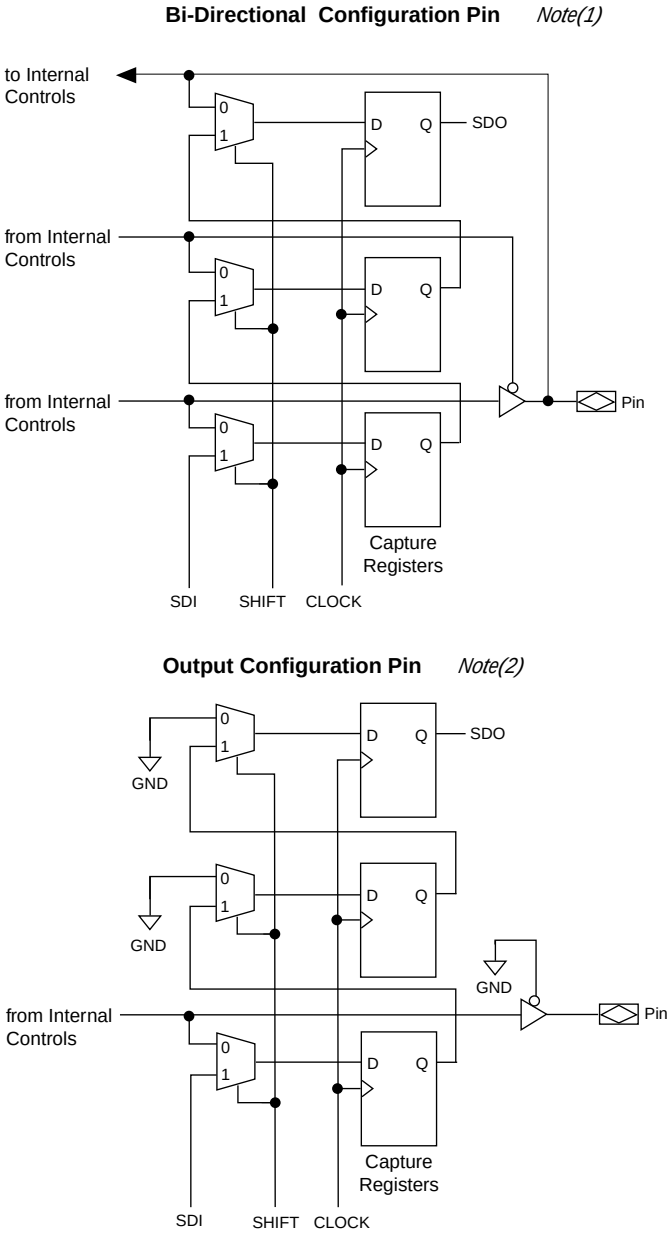


Notes:

(1) For FLEX 10K devices, these pins include nCONFIG, MSELØ, MSEL1, nCE, and DCLK; for FLEX 8000 devices, these pins include nCONFIG, nSP, MSELØ, and MSEL1, and for FLEX 6000 devices, these pins include nCONFIG, MSEL, nCE, and DCLK.

(2) For FLEX 10K, FLEX 8000, and FLEX 6000 devices, these pins include CONF_DONE and nSTATUS.

Figure 10. FLEX Dedicated Configuration Pins with IEEE 1149.1 BST Circuitry (Part 2 of 2)



Notes:

(1) For FLEX 8000 devices, these pins include DCLK and DATA.

(2) For FLEX 10K and FLEX 6000 devices, these pins include nCEO.

IEEE 1149.1 BST Operation Control

Altera IEEE 1149.1 devices implement the following BST instructions: SAMPLE/PRELOAD, EXTEST, BYPASS, UESCODE, and IDCODE. Table 4 summarizes the BST instructions, which are described in detail later in this application note.

Table 4. Boundary-Scan Instructions

Mode	Instruction Code				Description
	FLEX 10K	FLEX 8000 FLEX 6000	MAX 9000 MAX 9000A	MAX 7000S MAX 7000A	
SAMPLE/ PRELOAD	0001010101	101	0001010101	0001010101 *Note (1)*	Allows a snapshot of the signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins.
EXTEST	0000000000	000	0000000000	000000000 *Note (1)*	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	1111111111	111	1111111111	1111111111 *Note (1)*	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through the selected device to adjacent devices during normal device operation.
UESCODE	0000000111 *Note (2)*	–	–	*Note (2)*	Selects the UESCODE register and places it between TDI and TDO, allowing the UESCODE to be serially shifted out of TDO.
IDCODE	0000000110	–	0001011001 *Note (3)*	0001011001	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.

Notes to table:

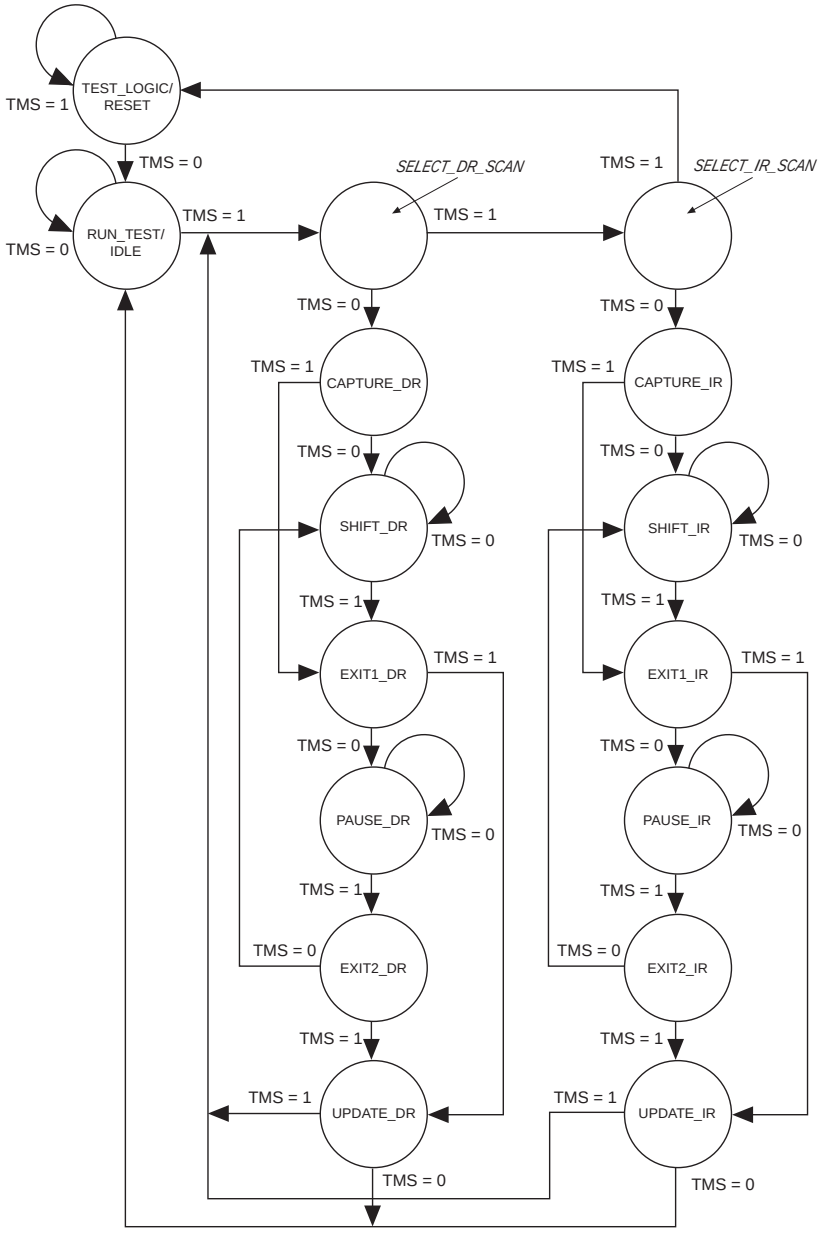
(1) EPM7032S, EPM7064S, and EPM7096S devices do not support IEEE 1149.1 BST. However, these devices have a BYPASS mode that allows them to pass IEEE 1149.1 information to other devices in the scan chain that support IEEE 1149.1 BST.

(2) FLEX 10K and MAX 7000S devices have private instructions to read the UESCODE register. The FLEX 10K UESCODE register is 7 bits long. The MAX 7000S UESCODE register is 16 bits long.

(3) IDCODE is available in all MAX 9000 (including MAX 9000A) devices except in early revisions of EPM9320 and EPM9560 devices.

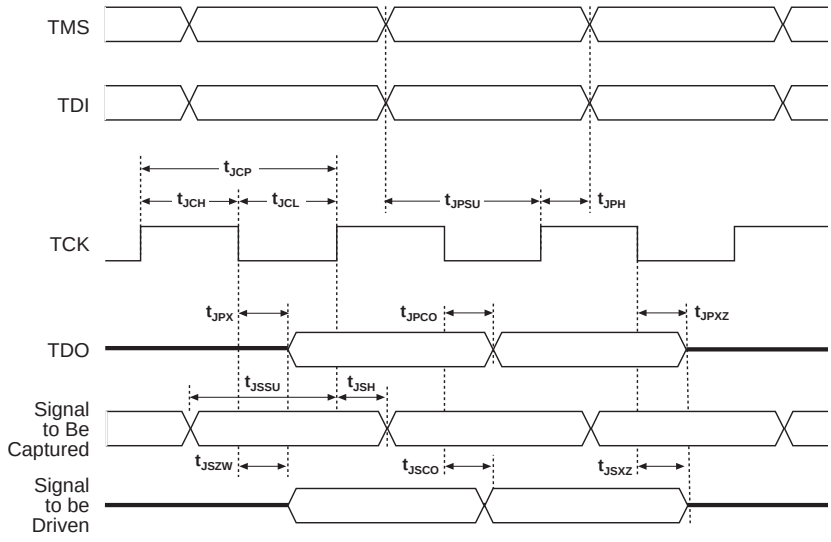
The IEEE 1149.1 test access port (TAP) Controller, a 16-state state machine clocked on the rising edge of TCK, uses the TMS pin to control IEEE 1149.1 operation in the device. Figure 11 shows the TAP Controller state machine.

Figure 11. IEEE 1149.1 TAP Controller State Machine



When the TAP controller is in the TEST_LOGIC/RESET state, the BST circuitry is disabled, the device is in normal operation, and the instruction register is initialized. If the device supports IDCODE, this initial instruction is IDCODE; otherwise, it is BYPASS. At device power-up, the TAP controller starts in this TEST_LOGIC/RESET state. In addition, the TAP controller may be forced to the TEST_LOGIC/RESET state by holding TMS high for five TCK clock cycles or by holding the TRST pin low (if the optional TRST pin is supported.) Once in the TEST_LOGIC/RESET state, the TAP controller remains in this state as long as TMS continues to be held high while TCK is clocked or TRST continues to be held low. Figure 12 shows the timing requirements for the IEEE 1149.1 signals.

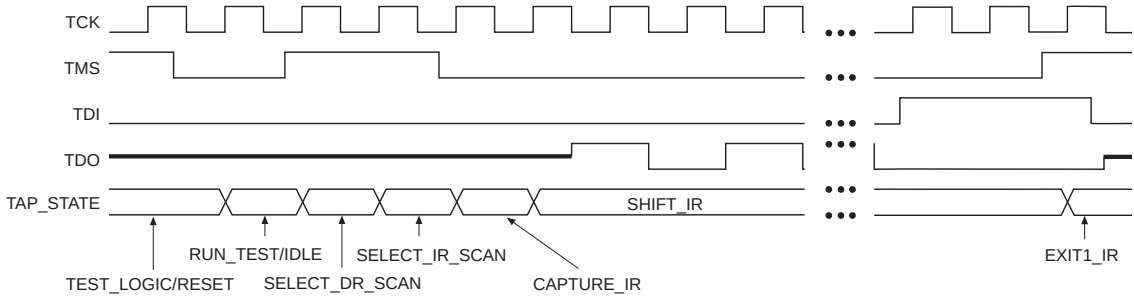
Figure 12. IEEE 1149.1 Timing Waveforms



The timing values for each Altera device are provided in the appropriate device family data sheet.

To start IEEE 1149.1 operation, select an instruction mode by advancing the TAP Controller to the shift instruction register (SHIFT_IR) state and shift in the appropriate instruction code on the TDI pin. The waveform diagram in Figure 13 represents the entry of the instruction code into the instruction register. It shows the values of TCK, TMS, TDI, and TDO and the states of the TAP Controller. From the RESET state, TMS is clocked with the pattern 01100 to advance the TAP Controller to SHIFT_IR.

Figure 13. Selecting the Instruction Mode



The TDO pin is tri-stated in all states except in the SHIFT_IR and SHIFT_DR states. The TDO pin is activated at the first falling edge of TCK after entering either of the shift states and is tri-stated at the first falling edge of TCK after leaving either of the shift states.

When the SHIFT_IR state is activated, TDO is no longer tri-stated, and the initial state of the instruction register is shifted out on the falling edge of TCK. TDO continues to shift out the contents of the instruction register as long as the SHIFT_IR state is active. The TAP Controller remains in the SHIFT_IR state as long as TMS remains low.

During the SHIFT_IR state, an instruction code is entered by shifting data on the TDI pin on the rising edge of TCK. The last bit of the opcode must be clocked at the same time that the next state, EXIT1_IR, is activated; EXIT1_IR is entered by clocking a logic high on TMS. Once in the EXIT1_IR state, TDO becomes tri-stated again. TDO is always tri-stated except in the SHIFT_IR and SHIFT_DR states. After an instruction code is entered correctly, the TAP Controller advances to perform the serial shifting of test data in one of three modes—SAMPLE / PRELOAD, EXTEST, or BYPASS—that are described below.

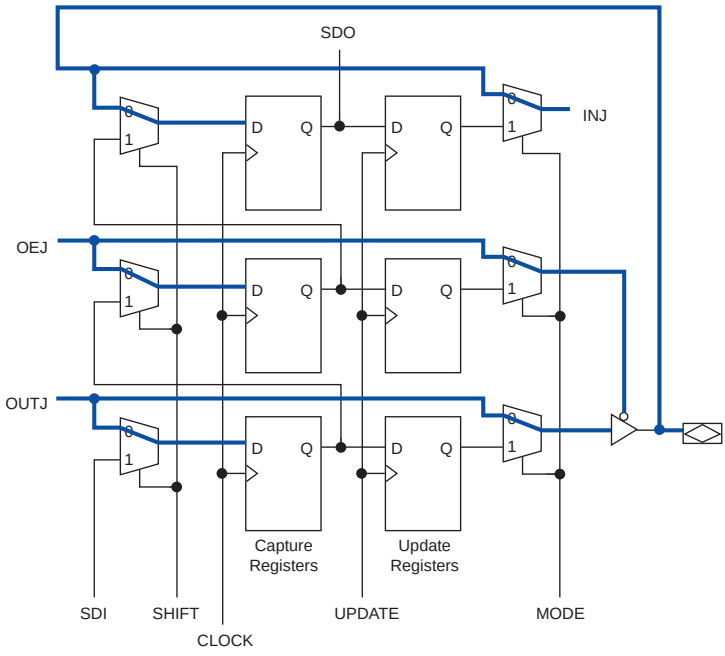
SAMPLE/PRELOAD Instruction Mode

The SAMPLE / PRELOAD instruction mode allows you to take a snapshot of device data without interrupting normal device operation. Figure 14 shows the capture, shift, and update phases of the SAMPLE / PRELOAD mode.

Figure 14. IEEE 1149.1 BST SAMPLE/PRELOAD Mode

Capture Phase

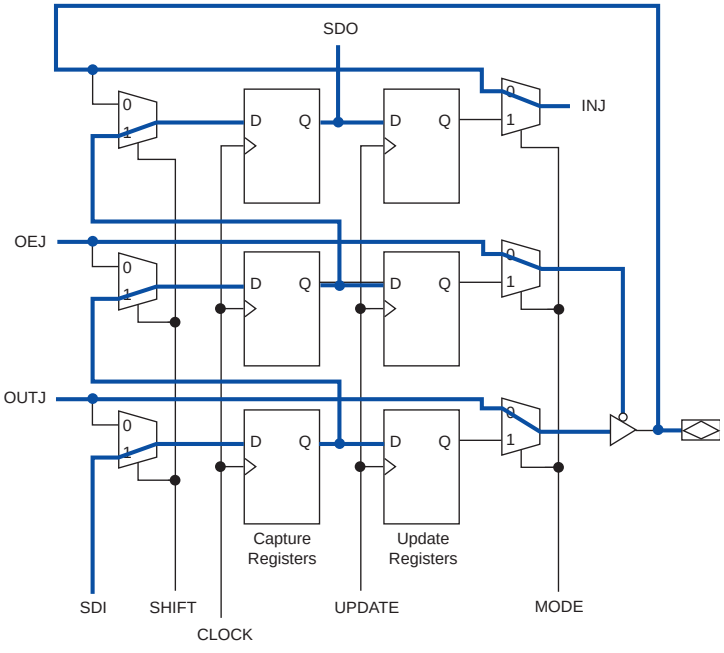
In the capture phase, the signals at the pin, OEJ and OUTJ, are loaded into the capture registers. The register CLOCK signal is supplied by the TAP Controller's CLOCKDR output. The data retained in these registers consists of signals from normal device operation.



Shift & Update Phases

In the shift phase, the previously captured signals at the pin, OEJ and OUTJ, are shifted out of the boundary-scan register via the TDO pin using CLOCK. As data is shifted out, the patterns for the next test can be shifted in via the TDI pin.

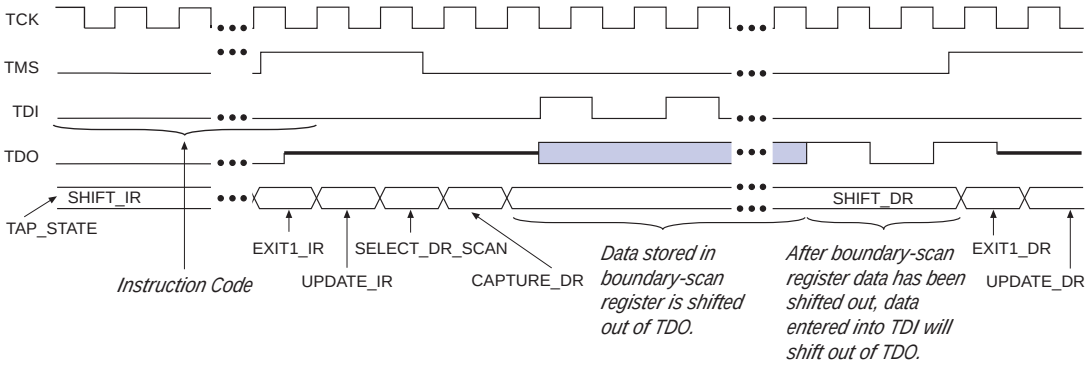
In the update phase, data is transferred from the capture registers to the UPDATE registers using the UPDATE Clock. The data stored in the UPDATE registers can be used for the EXTEST instruction.



During the capture phase, the multiplexers that precede the capture registers select the active device data signals; this data is then clocked into the capture registers. The multiplexers at the outputs of the update registers also select active device data to prevent functional interruptions to the device. During the shift phase, the boundary-scan shift register is formed by clocking data through capture registers around the device periphery and then out of the TDO pin. New test data can simultaneously be shifted into TDI and replace the contents of the capture registers. During the update phase, data in the capture registers is transferred to the update registers. This data can then be used in the EXTEST instruction mode. Refer to "EXTEST Instruction Mode" on page 237 for more information.

Figure 15 shows the SAMPLE / PRELOAD waveforms. The SAMPLE / PRELOAD instruction code is shifted in through the TDI pin. The TAP Controller advances to the CAPTURE_DR state and then to the SHIFT_DR state, where it remains if TMS is held low. The data shifted out of the TDO pin consists of the data that was present in the capture registers after the capture phase. New test data shifted into the TDI pin appears at the TDO pin after being clocked through the entire boundary-scan register. Figure 15 shows that the instruction code at TDI does not appear at the TDO pin until after the capture register data is shifted out. If TMS is held high on two consecutive TCK clock cycles, the TAP Controller advances to the UPDATE_DR state for the update phase.

Figure 15. SAMPLE/PRELOAD Shift Data Register Waveforms



EXTEST Instruction Mode

The EXTEST instruction mode is used primarily to check external pin connections between devices. Unlike the SAMPLE / PRELOAD mode, EXTEST allows test data to be forced onto the pin signals. By forcing known logic high and low levels on output pins, opens and shorts can be

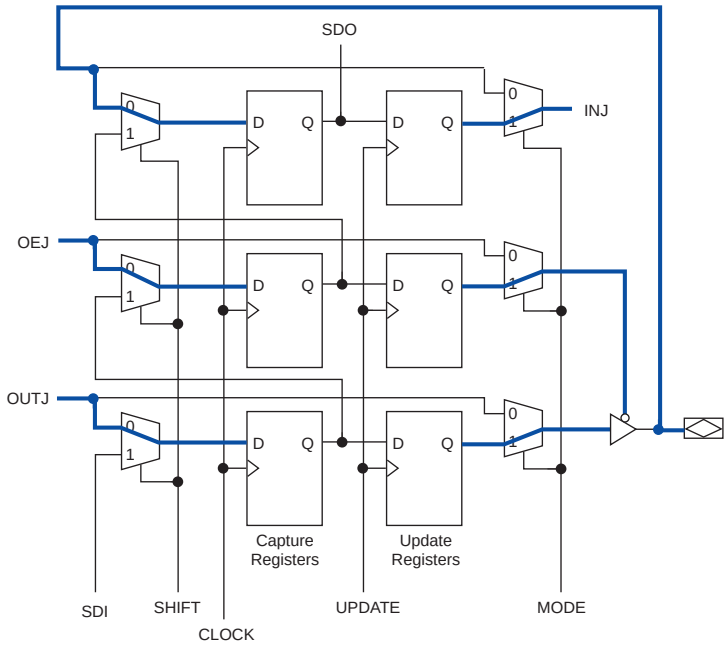
detected at pins of any device in the scan chain. Figure 16 shows the capture, shift, and update phases of the EXTEST mode.

Figure 16. IEEE 1149.1 BST EXTEST Mode

Capture Phase

In the capture phase, the signals at the pin, OEJ and OUTJ, are loaded into the capture registers. The register CLOCK signal is supplied by the TAP Controller's CLOCKDR output. Previously retained data in the update registers drives the IOC input, INJ, and allows the I/O pin to tri-state or drive a signal out.

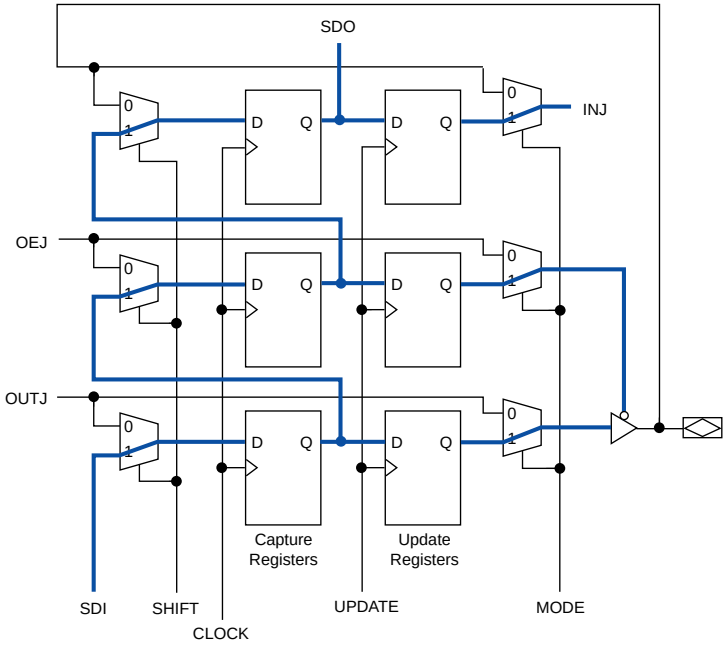
A "1" in the OEJ update register tri-states the output buffer.



Shift & Update Phases

In the shift phase, the previously captured signals at the pin, OEJ and OUTJ, are shifted out of the boundary-scan register via the TDO pin using CLOCK. As data is shifted out, the patterns for the next test can be shifted in via the TDI pin.

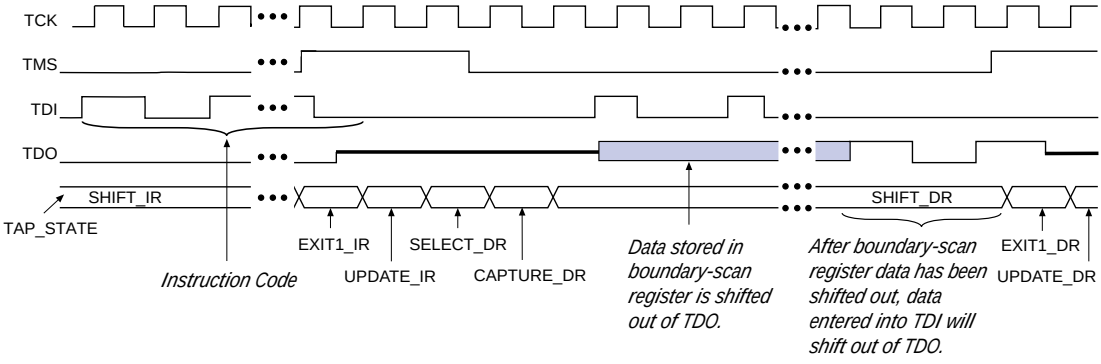
In the update phase, data is transferred from the capture registers to the update registers using the UPDATE Clock. The update registers then drive the IOC input, INJ, and allow the I/O pin to tri-state or drive a signal out.



EXTEST selects data differently than SAMPLE/PRELOAD. EXTEST chooses data from the update registers as the source of the INJ, output, and output enable signals. Once the EXTEST instruction code is entered, the multiplexers select the update register data; thus, data stored in these registers from a previous EXTEST or SAMPLE/PRELOAD test cycle can be forced onto the pin signals. In the capture phase, the results of this test data are stored in the capture registers and then shifted out of TDO during the shift phase. New test data can then be stored in the update registers during the update phase.

The waveform diagram in Figure 17 resembles the SAMPLE/PRELOAD waveform diagram, except that the instruction code for EXTEST uses all zeros. The data shifted out of TDO consists of the data that was present in the capture registers after the capture phase. New test data shifted into the TDI pin appears at the TDO pin after being clocked through the entire boundary-scan register.

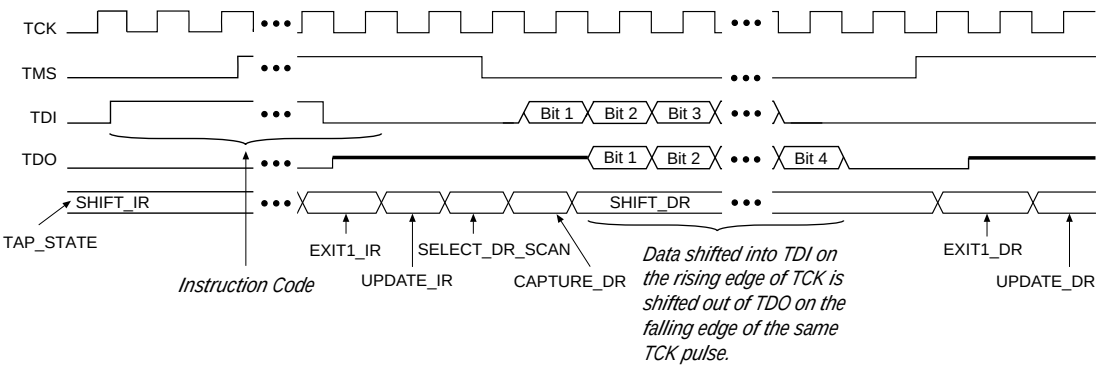
Figure 17. EXTEST Shift Data Register Waveforms



BYPASS Instruction Mode

The BYPASS instruction mode is activated with an instruction code made up of only ones. The waveforms in Figure 18 show how scan data passes through a device once the TAP Controller is in the SHIFT_DR state. In this state, data signals are clocked into the bypass register from TDI on the rising edge of TCK and out of TDO on the falling edge of the same clock pulse.

Figure 18. BYPASS Shift Data Register Waveforms



UESCODE Instruction Mode

The UESCODE instruction mode is used to examine the user electronic signature (UES) within the devices along a IEEE 1149.1 chain. When this instruction is selected, the UES register is connected between the TDI and TDO ports and the user-defined UES is shifted out through the UES register.

In FLEX 10K devices, the UES register is 7 bits long, and in MAX 7000S devices, it is 16 bits long.

☞ Although both this UESCODE instruction and the optional IEEE 1149.1 USERCODE instruction provide the ability to read out a user-defined UES, UES is shifted out in different ways.

IDCODE Instruction Mode

The IDCODE instruction mode is used to perform a blind interrogation of the devices in a IEEE 1149.1 chain. When IDCODE is selected, the device identification register is loaded with the 32-bit vendor-defined identification code and connected between the TDI and TDO ports. The 32-bit vendor-defined identification register for Altera devices is listed in Table 5.

Table 5. IDCODE for Altera Devices

Device	IDCODE, *Note (1)*			
	Version (4 bits)	Part Number (16 bits)	Manufacturer's Identity (11 bits)	1 (1 Bit)
EPF10K10, EPF10K10A	0000	0001 0000 0001 0000	00001101110	1
EPF10K20	0000	0001 0000 0010 0000	00001101110	1
EPF10K30, EPF10K30A	0000	0001 0000 0011 0000	00001101110	1
EPF10K50, EPF10K50V	0000	0001 0000 0101 0000	00001101110	1
EPF10K70	0000	0001 0000 0111 0000	00001101110	1
EPF10K100, EPF10K100A	0000	0000 0001 0000 0000	00001101110	1
EPF10K130V	0000	0000 0001 0011 0000	00001101110	1
EPF10K250A	0000	0000 0010 0101 0000	00001101110	1
EPM9320A	0000	1001 0011 0010 0000	00001101110	1
EPM9400	0000	1001 0100 0000 0000	00001101110	1
EPM9480, EPF9480A	0000	1001 0100 1000 0000	00001101110	1
EPM9560A	0000	1001 0101 0110 0000	00001101110	1
EPM7032S	0000	0111 0000 0011 0010	00001101110	1
EPM7064S	0000	0111 0000 0110 0100	00001101110	1
EPM7128S, EPM7128A	0000	0111 0001 0010 1000	00001101110	1
EPM7160S	0000	0111 0001 0110 0000	00001101110	1
EPM7192S	0000	0111 0001 1001 0010	00001101110	1
EPM7256S, EPM7256A	0000	0111 0010 0101 0110	00001101110	1

Note:
(1) The most significant bit (MSB) is on the left.

Enabling IEEE 1149.1 BST Circuitry

The IEEE 1149.1 BST circuitry for Altera devices is enabled upon device power-up. Because this circuitry may be used for BST, ISP, or ICR (depending in the device), this circuitry must be enabled only at specific times. This section describes how to enable the IEEE 1149.1 circuitry when needed and to ensure that the circuitry is not inadvertently enabled when it is not needed.

FLEX 10K & MAX 9000 Devices

The IEEE 1149.1 BST circuitry for Altera devices is enabled upon device power-up. You can use IEEE 1149.1 BST both before and after device programming or configuration. Because these devices have dedicated IEEE 1149.1 pins, their BST circuitry is always enabled. To disable the JTAG circuitry in these devices, tie these pins to the values shown in Table 6.

Table 6. Disabling IEEE 1149.1 Circuitry

Device	Compiler Option	JTAG Pins, *Note (1)*				
		TMS	TCK	TDI	TDO	TRST
FLEX 10K	–	VCC	VCC	VCC	Leave open	GND
FLEX 8000	JTAG Disabled	User I/O	User I/O	User I/O	User I/O	GND
	JTAG Enabled	VCC	VCC	VCC	Leave open	GND
FLEX 6000	JTAG Disabled	User I/O	User I/O	User I/O	User I/O	–
	JTAG Enabled	VCC	VCC	VCC	Leave open	–
MAX 9000	–	VCC	VCC	VCC	Leave open	–
MAX 7000S	JTAG Disabled	User I/O	User I/O	User I/O	User I/O	–
	JTAG Enabled	VCC	VCC	VCC	Leave open	–

Note:
(1) If the design has been compiled with IEEE 1149.1 circuitry enabled, tying the IEEE 1149.1 pins to the appropriate state will deactivate the IEEE 1149.1 circuitry.

FLEX 8000 & FLEX 6000 Devices

The IEEE 1149.1 BST circuitry for Altera devices is enabled upon device power-up. You can use BST both before and after device programming or configuration. In FLEX 8000 and FLEX 6000 devices, if the dedicated configuration pin nCONFIG is held low, configuration is delayed and you can perform BST.

Because these devices have four pins that can be used as either JTAG pins or user I/O pins, you must enable or disable the JTAG circuitry before compilation. For a design that has been compiled with JTAG pins enabled, the four pins operate as dedicated pins only. If these devices are not using the IEEE 1149.1 circuitry, tying the pins to the appropriate state (shown in Table 6) disables the circuitry.

By choosing **Device Options** from the **Device** dialog box (Assign menu), you can enable or disable IEEE 1149.1 support for applicable devices on a device-by-device basis with the *Enable JTAG Support* option in the **FLEX 8000** or **FLEX 6000 Individual Device Options** dialog box. You can also enable JTAG support for all devices in a project by choosing **Global Project Device Options** (Assign menu) and selecting the *Enable JTAG Support* option in the **FLEX 8000** or **FLEX 6000 Global Project Device Options** dialog box.

MAX 7000S & MAX 7000A Devices

The IEEE 1149.1 BST circuitry of MAX 7000S and MAX 7000A devices is enabled by an IEEE 1149.1 enable bit within the device. A blank device will always have the BST circuitry enabled. The state of this enable bit may be set only by programming in the Altera MPU or third-party programmer. The state of the JTAG enable bit may not be changes using ISP via the IEEE 1149.1 port.

Because these devices have four pins that can be used as either JTAG pins or user I/O pins, you must enable or disable the JTAG circuitry before compilation. For a design that has been compiled with JTAG pins enabled, the four pins operate as dedicated pins only. If these devices are not using the IEEE 1149.1 circuitry, tying the pins to the appropriate state (shown in Table 6) disables the circuitry.

By choosing **Device Options** from the **Device** dialog box (Assign menu), you can enable or disable IEEE 1149.1 support for applicable devices on a device-by-device basis with the *Enable JTAG Support* option in the **MAX 7000S** or **MAX 7000A Individual Device Options** dialog box. You can also enable JTAG support for all devices in a project by choosing **Global Project Device Options** (Assign menu) and selecting the *Enable JTAG Support* option in the **MAX 7000S** or **MAX 7000A Global Project Device Options** dialog box.

Guidelines for IEEE 1149.1 Boundary-Scan Testing

Use the following guidelines when performing boundary-scan testing with IEEE 1149.1 devices:

- If the "10..." pattern does not shift out of the instruction register via the TDO pin during the first clock cycle of the SHIFT_IR state, the proper TAP Controller state has not been reached. To solve this problem, try one of the following procedures:
  - Verify that the TAP Controller has reached the SHIFT_IR state correctly. To advance the TAP Controller to the SHIFT_IR state, return to the RESET state and clock the code 01100 on the TMS pin.
  - Check the connections to the VCC, GND, JTAG, and dedicated configuration pins on the device.
  - For all FLEX and MAX 7000S devices, if the device is in user mode, make sure that you have turned on the *Enable JTAG Support* option in the MAX+PLUS II software.

- Perform a SAMPLE/PRELOAD test cycle prior to the first EXTEST test cycle to ensure that known data is present at the device pins when the EXTEST mode is entered. If the OEJ update register contains a 0, the data in the OUTJ update register will be driven out. The state must be known and correct to avoid contention with other devices in the system.
- Do not perform EXTEST and SAMPLE/PRELOAD during ISP or ICR. These instructions are supported before and after ISP/ICR but not during ISP and ICR.
- In FLEX 8000 devices, do not execute a BYPASS shift cycle before an EXTEST test cycle that requires preloaded test data. The bypass and boundary-scan registers shift simultaneously when the TAP Controller is in the SHIFT_DR state. Therefore, using the BYPASS mode will shift test data out of the capture registers.

If problems persist, contact Altera Applications at (800) 800-EPLD.

Boundary-Scan Description Language (BSDL) Support

The Boundary-Scan Description Language (BSDL)—a subset of VHDL—provides a syntax that allows you to describe the features of an IEEE 1149.1 BST-capable device that can be tested. Test software development systems can then use the BSDL files for test generation, analysis, failure diagnostics, and in-system programming. For more information, or to receive BSDL files for IEEE 1149.1-compliant Altera devices, contact Altera Applications.

Conclusion

The IEEE 1149.1 BST circuitry available in Altera devices provides a cost-effective and efficient way to test systems that contain devices with tight lead spacing. Circuit boards with Altera and other IEEE 1149.1-compliant devices can use the EXTEST, SAMPLE/PRELOAD, and BYPASS modes to create serial patterns that internally test the pin connections between devices and check device operation.

References

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